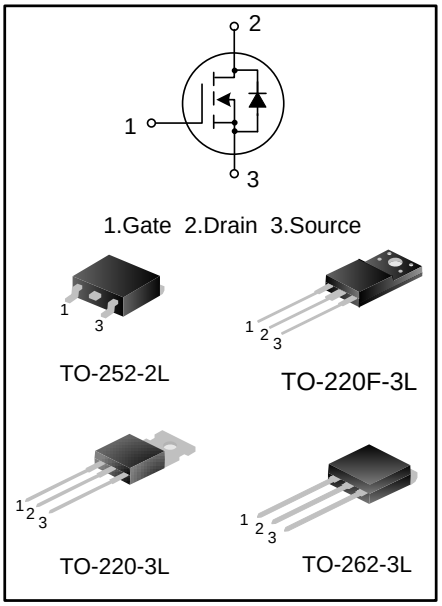
33A, 100V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD540T/D/K/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary new type of flat low-voltage structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

It can be widely used in electronic ballast, low-power SWPS.



FEATURES

- 33A,100V,$R_{DS(on)(typ.)}$=34mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVD540T	TO-220-3L	SVD540T	Pb free	Tube
SVD540DTR	TO-252-2L	SVD540D	Halogen free	Tape & Reel
SVD540K	TO-262-3L	SVD540K	Halogen free	Tube
SVD540F	TO-220F-3L	SVD540F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Rating				Unit
			SVD540T	SVD540D	SVD540K	SVD540F	
Drain-Source Voltage		V_{DS}	100				V
Gate-Source Voltage		V_{GS}	±20				V
Drain Current	T_C=25°C	I_D	33				A
	T_C=100°C		23				
Drain Current Pulsed		I_{DM}	110				A
Power Dissipation(T_C=25°C)		P_D	130	98	120	33	W
-Derate above 25°C			1.04	0.78	0.96	0.27	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	695.22				mJ
Operation Junction Temperature Range		T_J	-55～+150				°C
Storage Temperature Range		T_{stg}	-55～+150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating				Unit
		SVD540T	SVD540D	SVD540K	SVD540F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.96	1.28	1.04	3.77	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	100	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=Rated BV_{DSS}, V_{GS}=0V	--	--	25	μA
		V_{DS}=0.8 x Rated BV_{DSS}, V_{GS}=0V,T_C=125°C	--	--	250	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=16A	--	34	44	mΩ
Gate Resistance	R_g	f=1.0MHz	--	3.4	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	--	1239	--	pF
Output Capacitance	C_{oss}		--	247	--	
Reverse Transfer Capacitance	C_{rss}		--	44	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=16A, R_{GS}=5.1Ω, V_{GS}=10V	--	10	--	ns
Turn-on Rise Time	t_r		--	44	--	
Turn-off Delay Time	$t_{d(off)}$		--	46	--	
Turn-off Fall Time	t_f		--	13	--	
Total Gate Charge	Q_g	V_{DS}=80V, I_D=16A, V_{GS}=10V	--	37	--	nC
Gate-Source Charge	Q_{gs}		--	6.0	--	
Gate-Drain Charge	Q_{gd}		--	17	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	33	A
Pulsed Source Current	I_{SM}		--	--	110	
Diode Forward Voltage	V_{SD}	I_S=16A, V_{GS}=0V	--	--	1.2	V
Reverse Recovery Time	T_{rr}	I_S=33A, V_{GS}=0V dI$_F$/dt=100A/μs(Note 2)	--	98	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.4	--	nC

Notes:

1. L=1.5mH, I_{AS}=22.5A, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics(25°C)

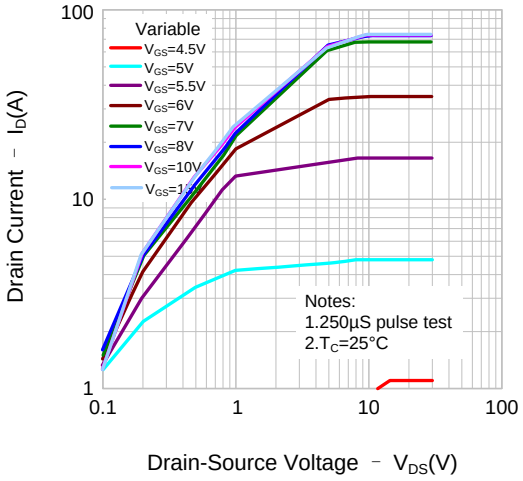


Figure 2. On-Region Characteristics(175°C)

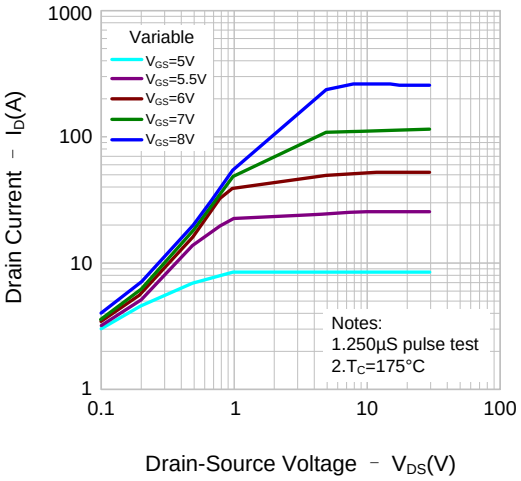


Figure 3. Transfer Characteristics

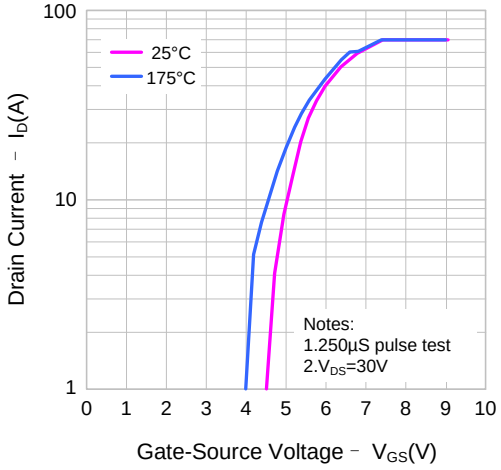


Figure 4. Source Drain Diode Forward Voltage Variation vs. Source Current and Temperature

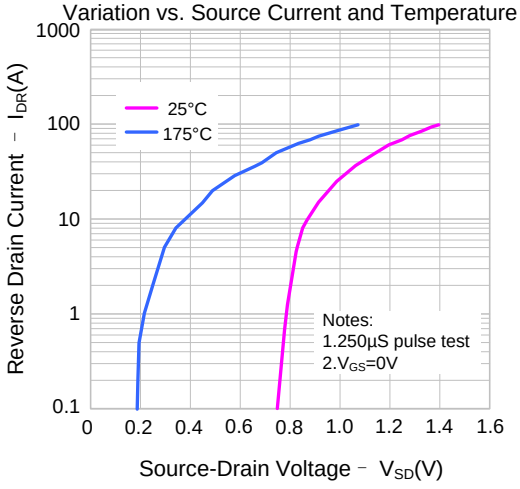


Figure 5. Capacitance Characteristics

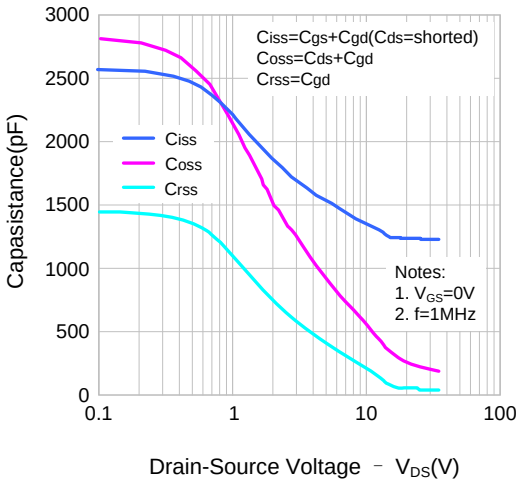
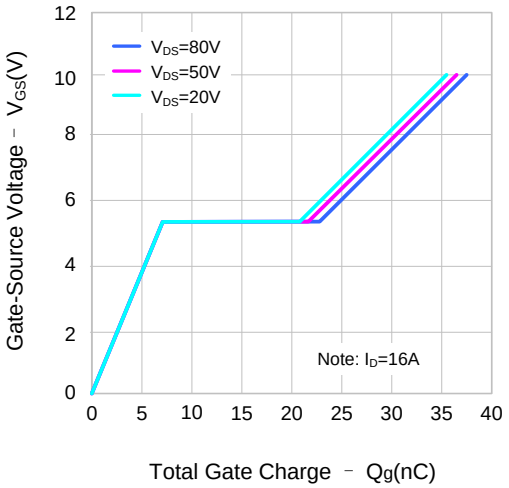


Figure 6. Gate Charge Characteristics



TYPICAL Characteristics

Figure 7. On-resistance Variation vs. Temperature

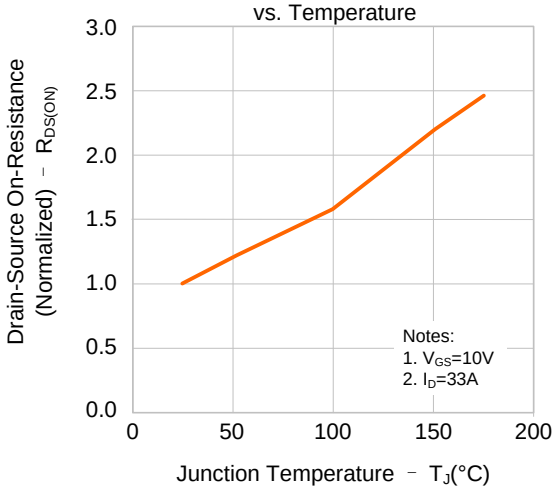


Figure 8-1. Max. Safe Operating Area(SVD540T)

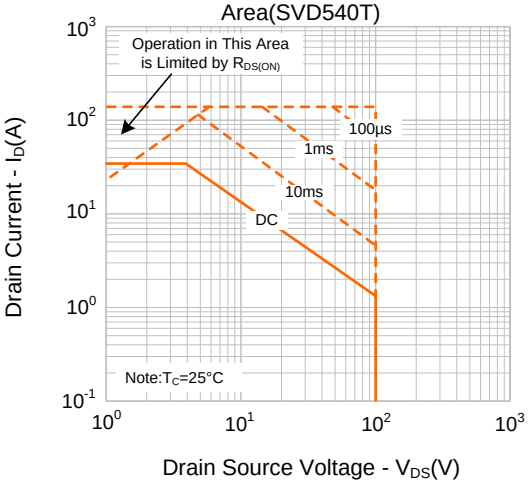


Figure 8-2. Max. Safe Operating Area(SVD540D)

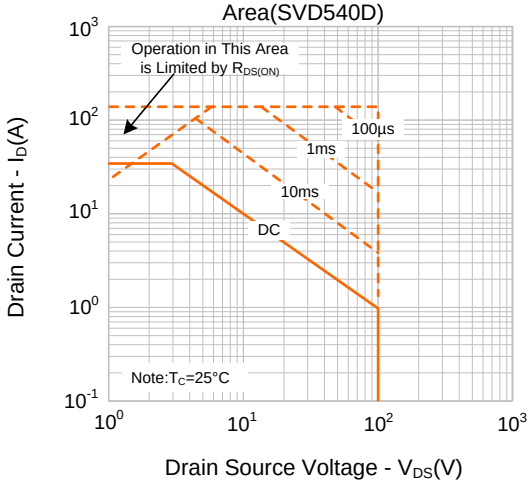


Figure 8-3. Max. Safe Operating Area(SVD540K)

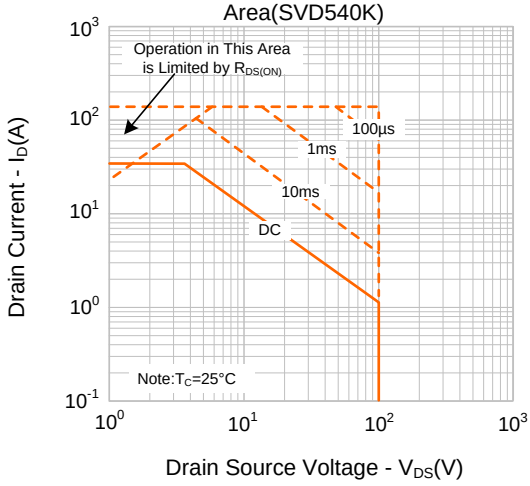


Figure 8-4. Max. Safe Operating Area(SVD540F)

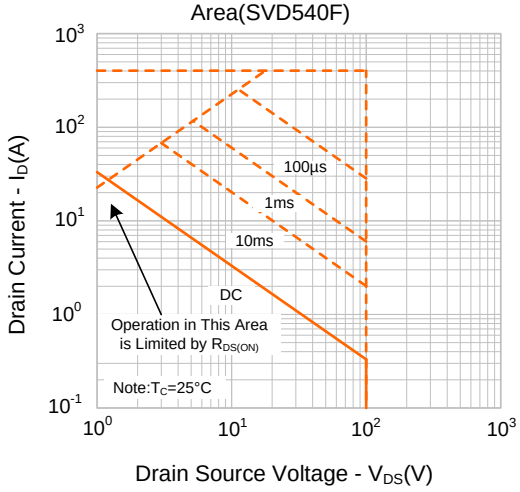
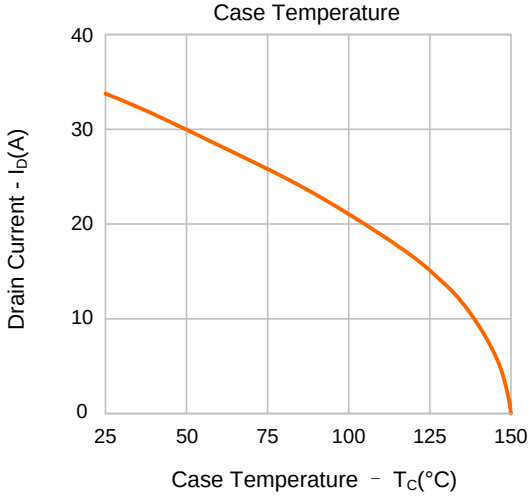
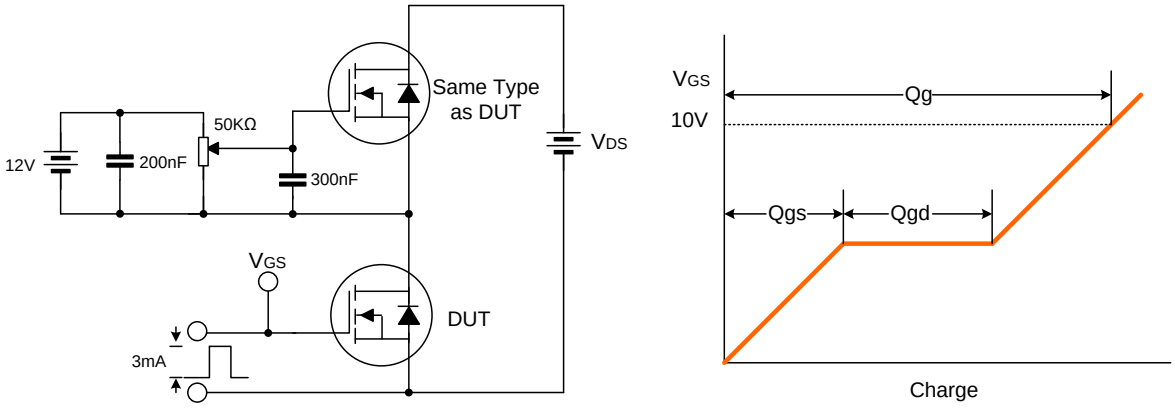


Figure 9. Maximum Drain Current vs. Case Temperature

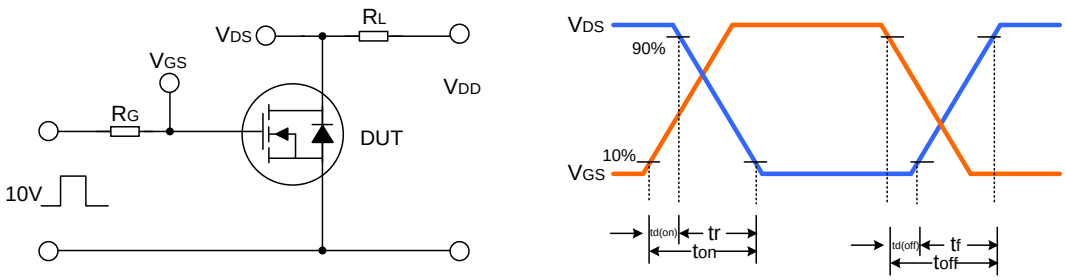


TYPICAL TEST CIRCUIT

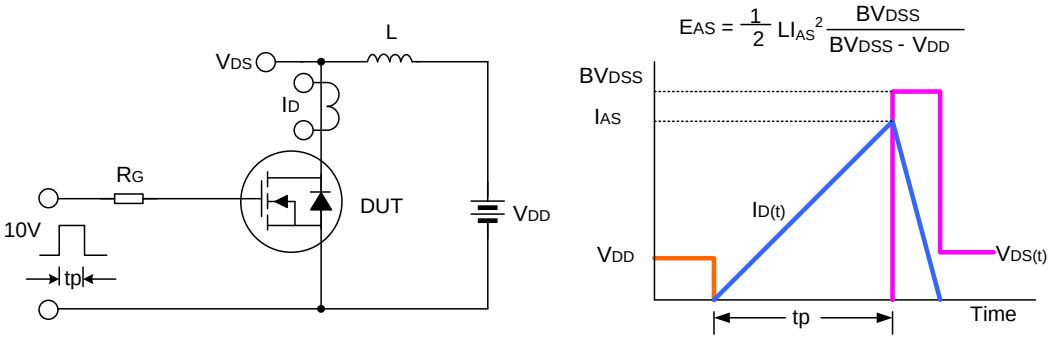
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



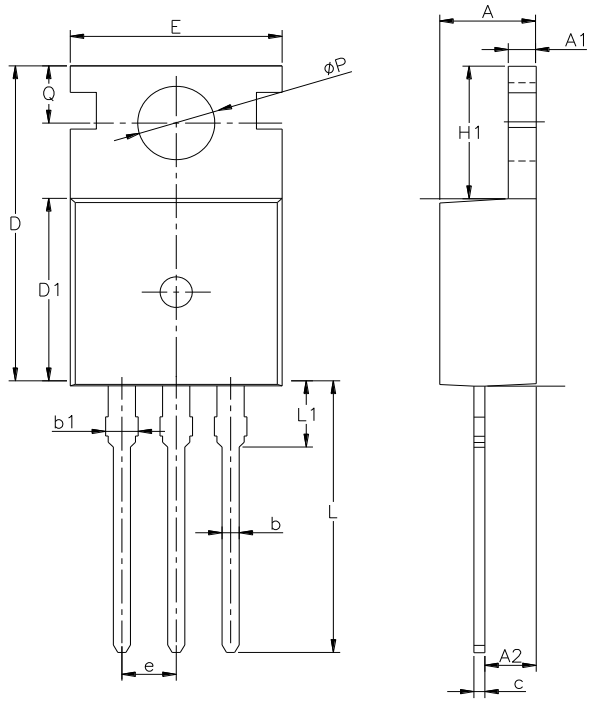
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220-3L

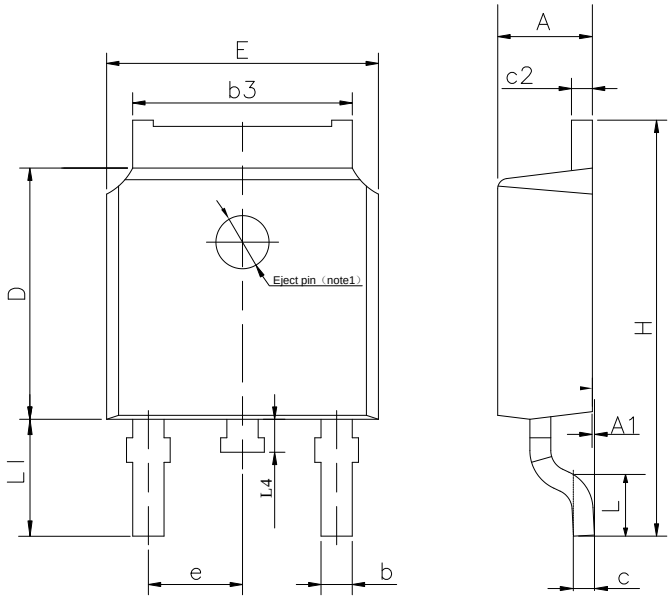
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ΦP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-252-2L

UNIT: mm



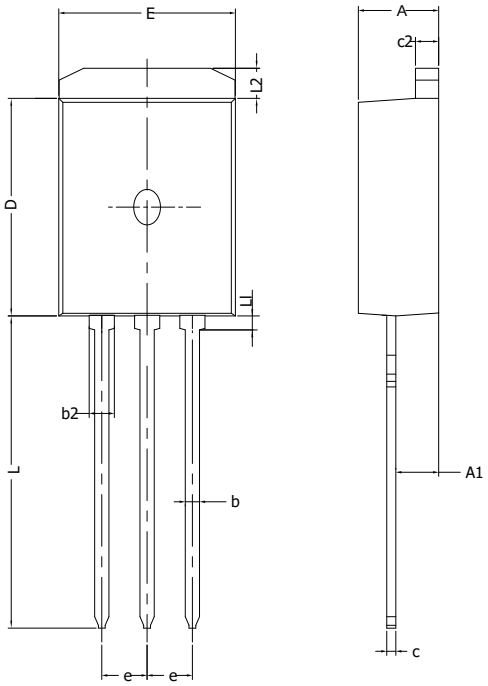
SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE

TO-262-3L

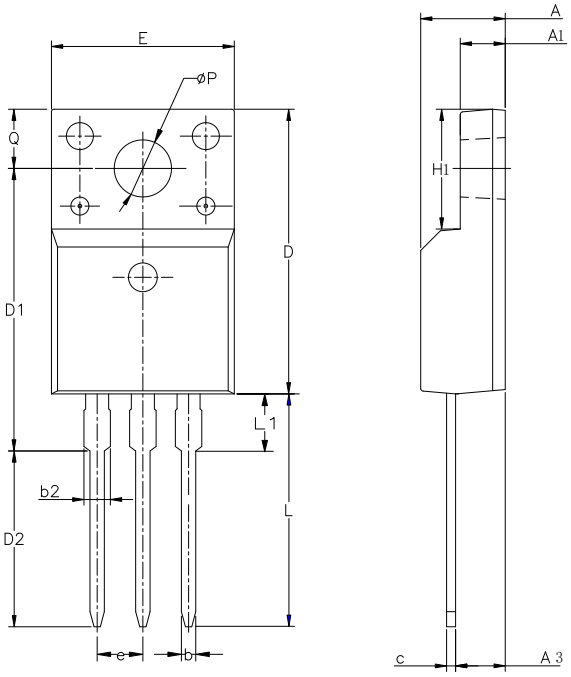
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	---	2.92
b	0.71	0.80	0.90
b2	1.20	---	1.50
c	0.34	---	0.65
c2	1.22	1.30	1.35
D	8.38	---	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	---	14.10
L1	---	---	0.75
L2	1.12	---	1.42

TO-220F-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Part No.:	SVD540T/D/K/F	Document Type:	Datasheet
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Rev.: 1.6

Revision History:

1. Add the package information of TO-220F-3L

Rev.: 1.5

Revision History:

1. Modify the package information of TO-252-2L
2. Modify the package information of TO-220-3L

Rev.: 1.4

Revision History:

1. Modify the thermal characteristics

Rev.: 1.3

Revision History:

1. Add the package of TO-262-3L

Rev.: 1.2

Revision History:

1. Add the package of TO-252-2L

Rev.: 1.1

Revision History:

1. Change the schematic diagram of MOS

Rev.: 1.0

Revision History:

1. First Release