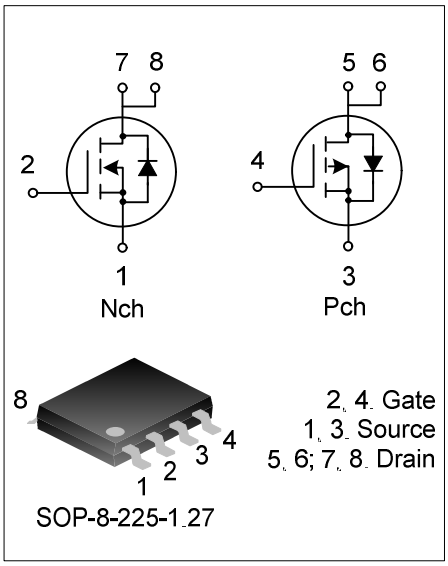
17A, 55V N/P-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD1055SA is a combination device packaged with an N-channel and a P-channel enhancement mode MOS FET, which is produced using Silan proprietary low-voltage planar VDMOS process. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.It's widely used in electronic ballasts and low power SMPS.



FEATURES

- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous substance control	Packing
SVD1055SA	SOP-8-225-1.27	SVD1055SA	Halogen free	Tube
SVD1055SATR	SOP-8-225-1.27	SVD1055SA	Halogen free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Rating		Unit
			N-ch	P-ch	
Drain-Source Voltage		V_{DS}	55	-55	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Drain Current	T_C=25°C	I_D	17	-12	A
	T_C=100°C		12	-8.5	
Drain Current Pulsed		I_{DM}	68	-48	A
Power Dissipation(T_C=25°C)		P_D	2.0		W
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	122	106	mJ
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

N channel

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	55	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=55V,V_{GS}=0V	--	--	1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}，I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=10A	--	45	70	mΩ
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1.0MHz	--	386	--	pF
Output Capacitance	C_{oss}		--	147	--	
Reverse Transfer Capacitance	C_{rss}		--	18	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=28V,V_{GS}=10V,R_G=25Ω, I_D=10A (Note 2, 3)	--	5.2	--	ns
Turn-on Rise Time	t_r		--	42	--	
Turn-off Delay Time	$t_{d(off)}$		--	26	--	
Turn-off Fall Time	t_f		--	16	--	
Total Gate Charge	Q_g	V_{DD}=44V, V_{GS}=10V, I_D=10A (Note 2, 3)	--	11	--	nC
Gate-Source Charge	Q_{gs}		--	2.9	--	
Gate-Drain Charge	Q_{gd}		--	3.8	--	
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	17	A
Pulsed Source Current	I_{SM}		--	--	68	
Diode Forward Voltage	V_{SD}	I_S=10A, V_{GS}=0V	--	--	1.3	V
Reverse Recovery Time	T_{rr}	I_S=10A, V_{GS}=0V, dI_F/dt=100A/μs (Note 2)	--	42	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.08	--	μc

Notes:

1. L=1mH, I_{AS}=13A, V_{DD}=25V, R_G=25Ω, starting temperature T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

P channel

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-55	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-55V,V_{GS}=0V	--	--	-1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS},I_D=-250μA	-2.0	--	-4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-7.2A	--	145	175	mΩ
Input Capacitance	C_{iss}	V_{DS}=-25V,V_{GS}=0V,f=1.0MHz	--	461	--	pF
Output Capacitance	C_{oss}		--	144	--	
Reverse Transfer Capacitance	C_{rss}		--	46	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-28V,V_{GS}=-10V,R_G=24Ω, I_D=-7.2A (Note 2, 3)	--	8.4	--	ns
Turn-on Rise Time	t_r		--	52	--	
Turn-off Delay Time	$t_{d(off)}$		--	35	--	
Turn-off Fall Time	t_f		--	27	--	
Total Gate Charge	Q_g	V_{DD}=-44V, V_{GS}=-10V, ID=-7.2A (Note 2, 3)	--	14	--	nC
Gate-Source Charge	Q_{gs}		--	2.8	--	
Gate-Drain Charge	Q_{gd}		--	5.8	--	
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	-12	A
Pulsed Source Current	I_{SM}		--	--	-48	
Diode Forward Voltage	V_{SD}	I_S=-7.2A, V_{GS}=0V	--	--	-1.6	V
Reverse Recovery Time	T_{rr}	I_S=-7.2A, V_{GS}=0V, dI_F/dt=100A/μs (Note 2)	--	54.33	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.101	--	μc

Notes:

1. L=1.0mH, I_{AS}= -8A, V_{DD}=25V, R_G=25Ω, starting temperature T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1-1. On-Region Characteristics (N-ch)

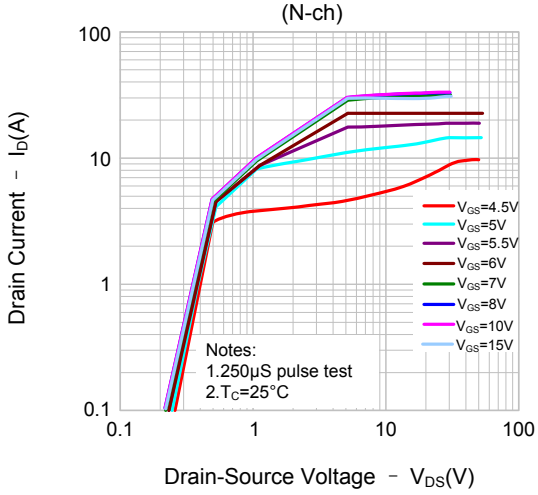


Figure 1-2. On-Region Characteristics (P-ch)

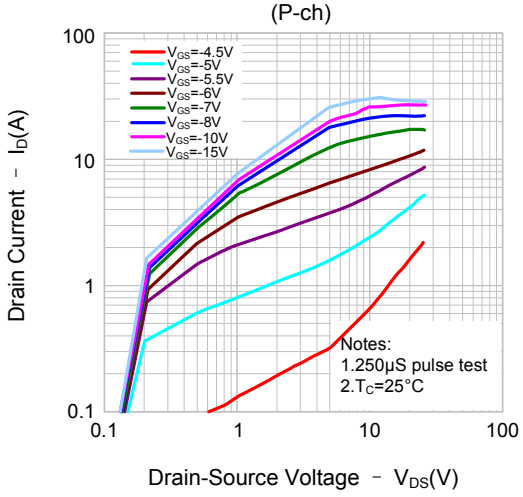


Figure 2-1. Transfer Characteristics (N-ch)

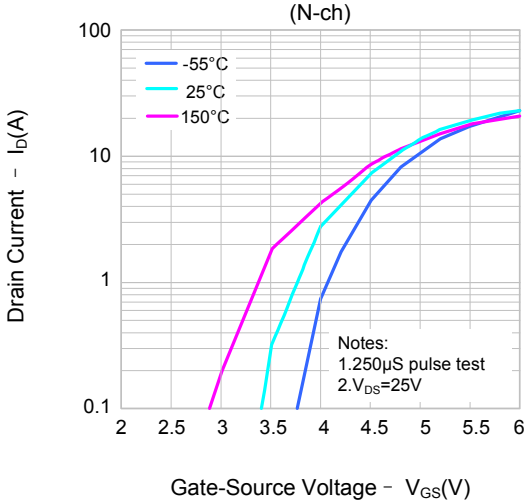


Figure 2-2. Transfer Characteristics (P-ch)

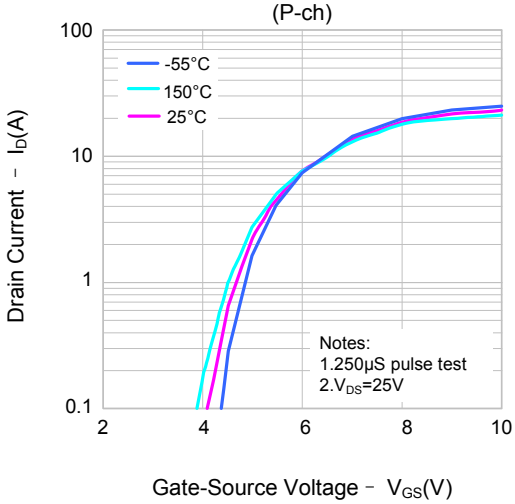


Figure 3-1. On-Resistance Variation vs. Drain Current and Gate Voltage (N-ch)

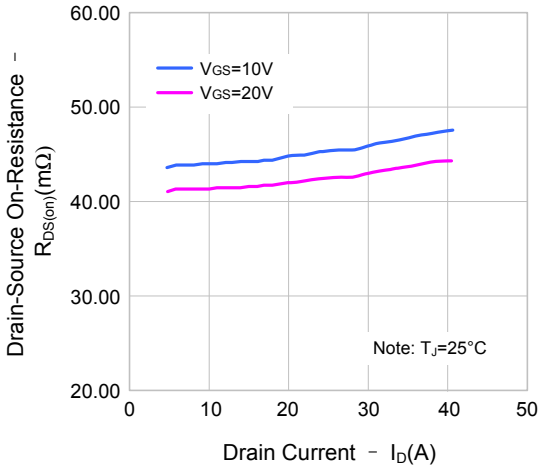
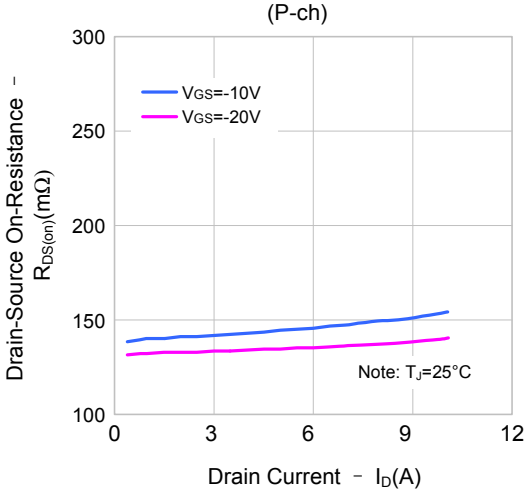


Figure 3-2. On-Resistance Variation vs. Drain Current and Gate Voltage (P-ch)



TYPICAL CHARACTERISTICS (continued)

Figure 4-1. Body Diode Forward Voltage Variation vs. Source Current and Temperature (N-ch)

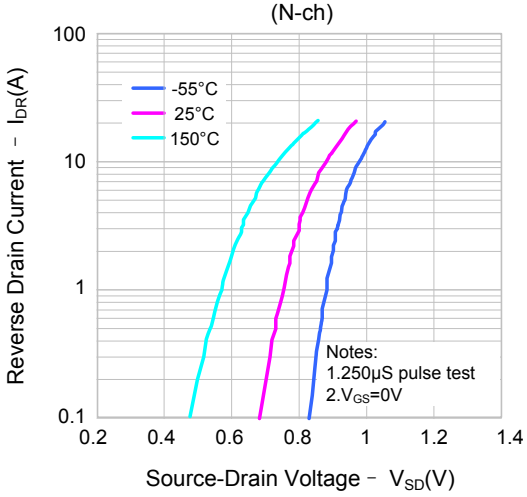


Figure 4-2. Body Diode Forward Voltage Variation vs. Source Current and Temperature (P-ch)

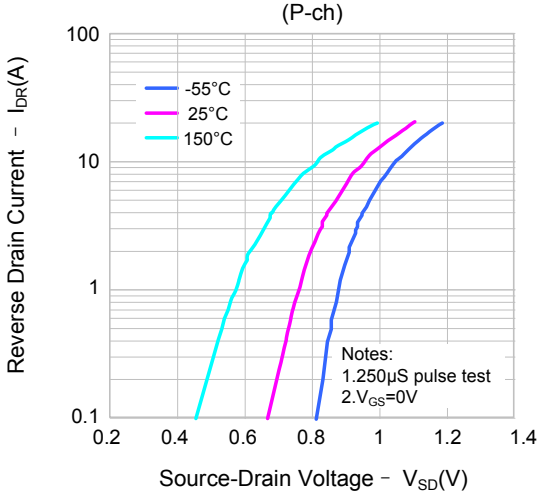


Figure 5-1. Capacitance Characteristics (N-ch)

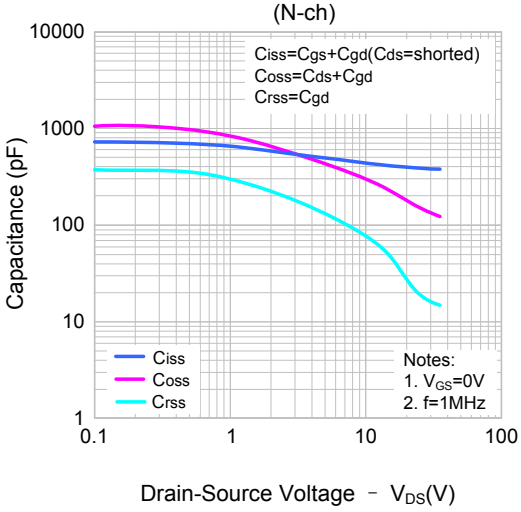


Figure 5-2. Capacitance Characteristics (P-ch)

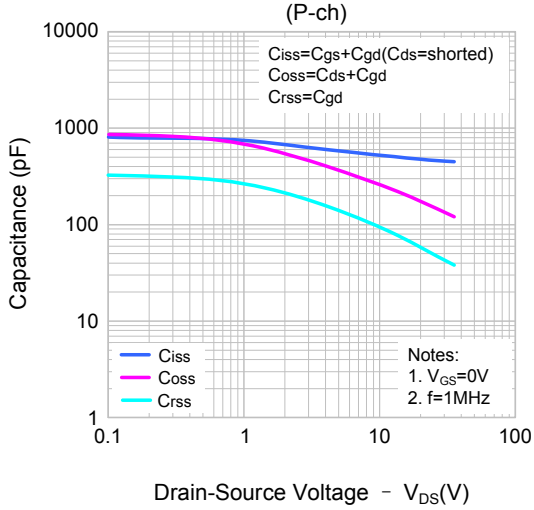


Figure 6-1. Gate Charge Characteristics (N-ch)

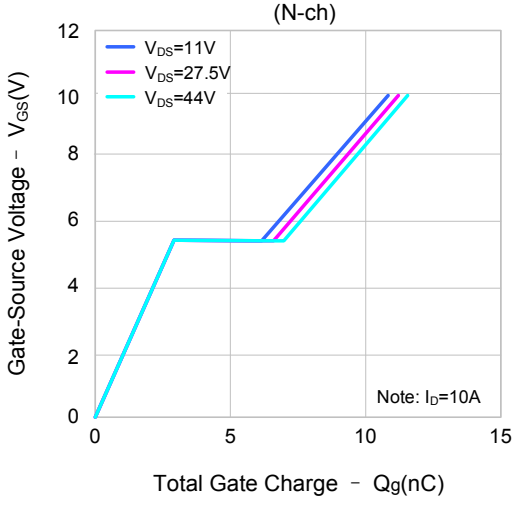
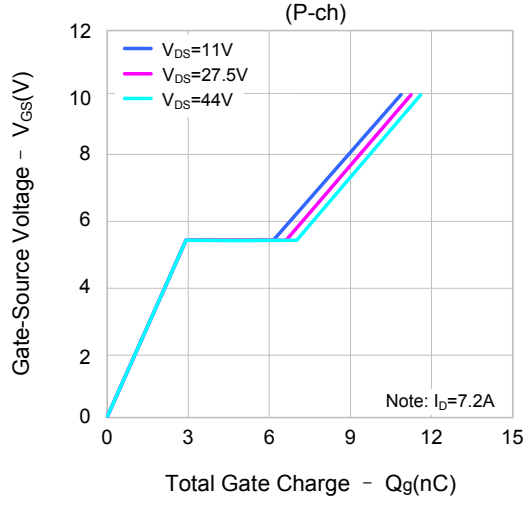


Figure 6-2. Gate Charge Characteristics (P-ch)



TYPICAL Characteristics (continued)

Figure 7-1. Breakdown Voltage Variation vs. Temperature (N-ch)

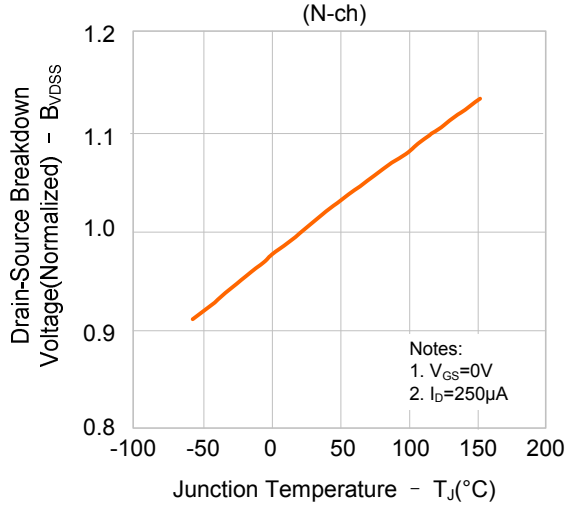


Figure 7-2. Breakdown Voltage Variation vs. Temperature (P-ch)

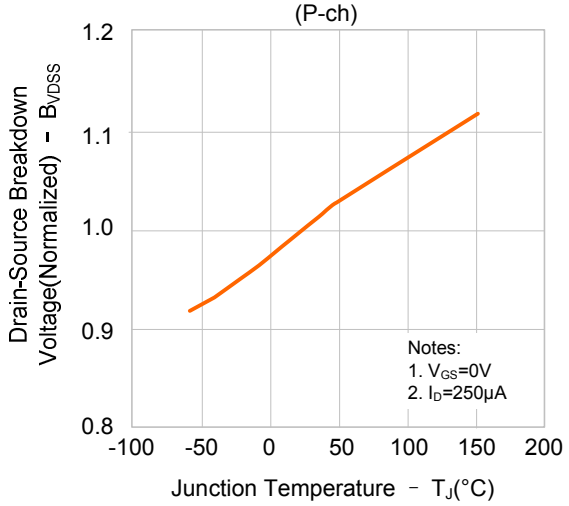


Figure 8-1. On-resistance Variation vs. Temperature (N-ch)

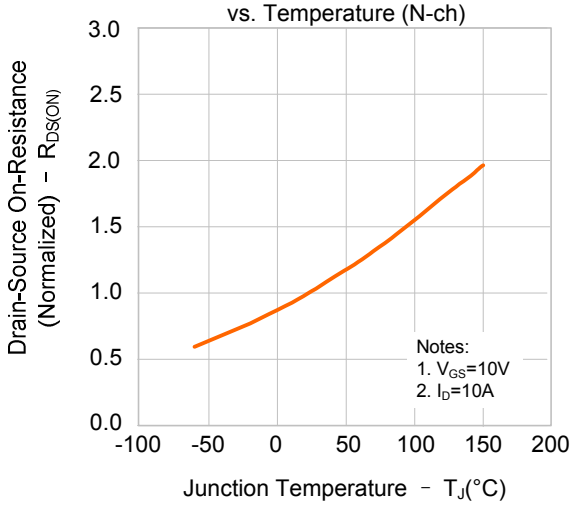


Figure 8-2. On-resistance Variation vs. Temperature (P-ch)

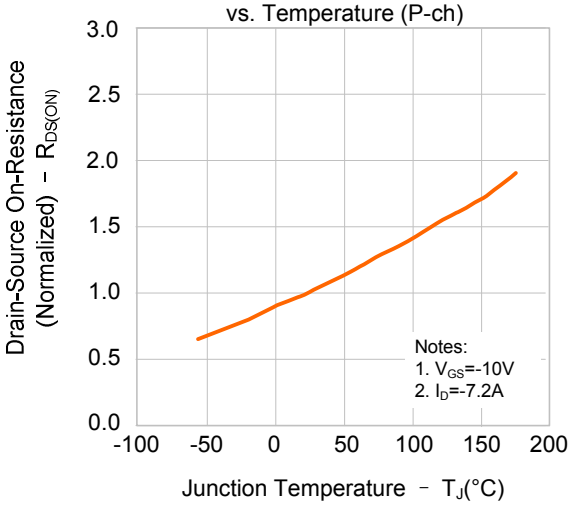


Figure 9-1. Max. Safe Operating Area (N-ch)

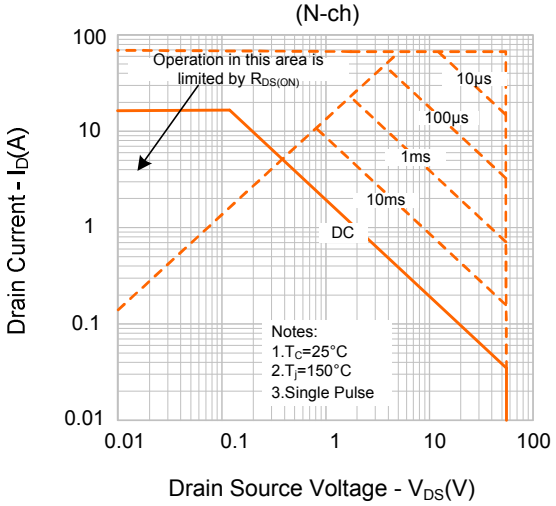
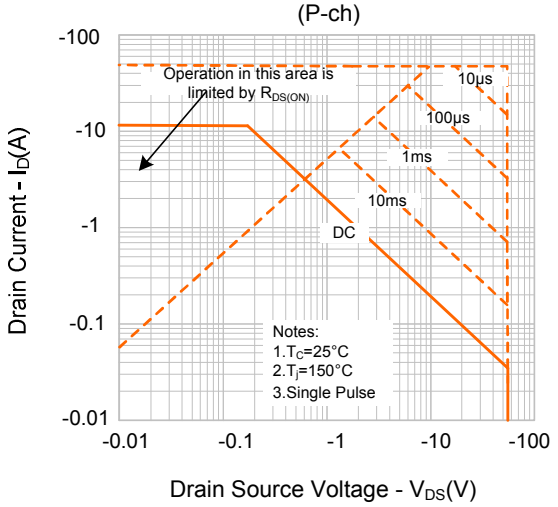
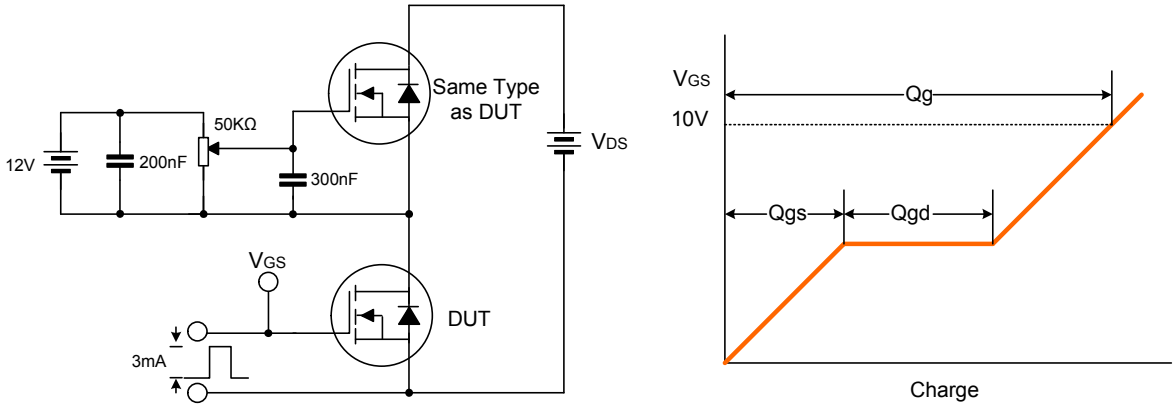


Figure 9-2. Max. Safe Operating Area (P-ch)

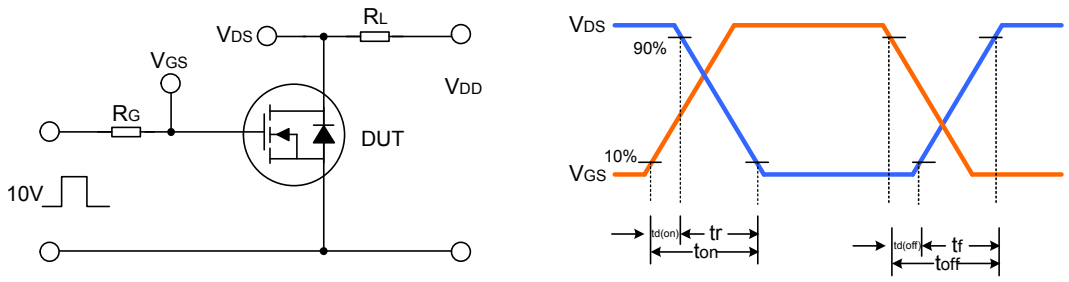


TYPICAL TEST CIRCUIT

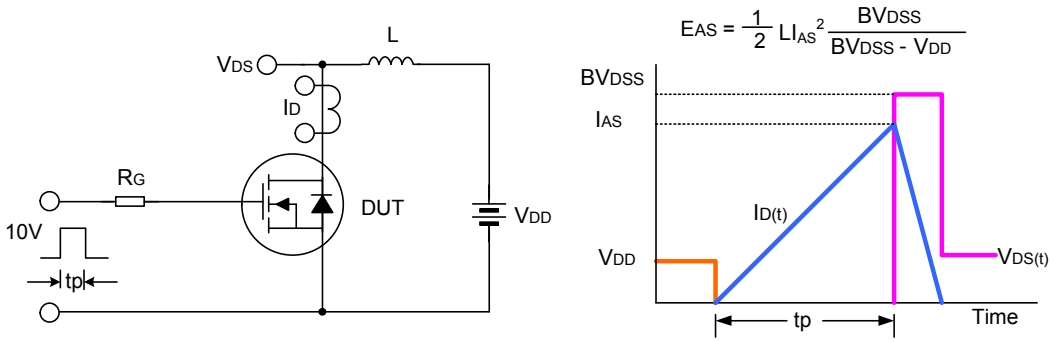
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

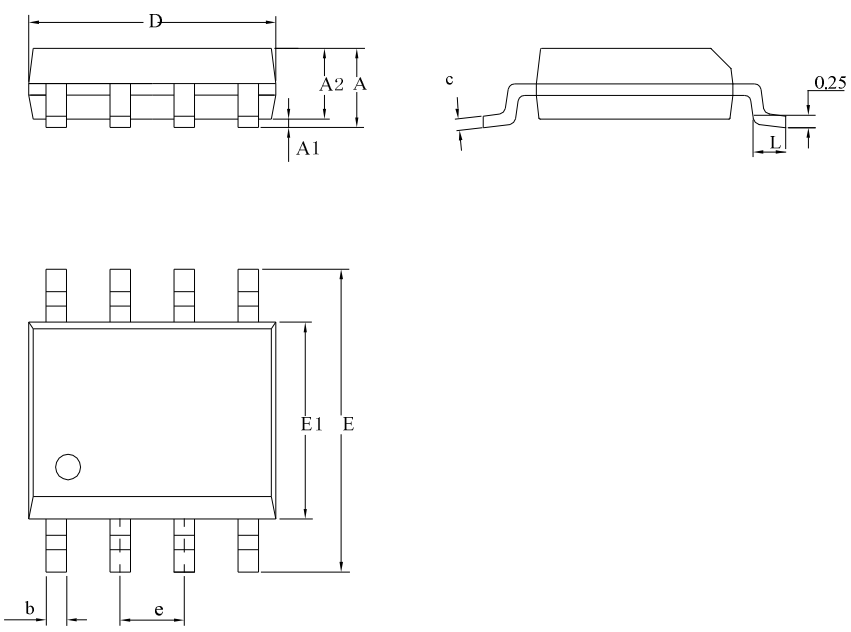


Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

SOP-8-225-1.27 **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	0.15	0.25
A2	1.25	--	1.65
b	0.32	0.42	0.52
c	0.15	0.2	0.26
D	4.70	4.90	5.30
E	5.60	6.00	6.40
E1	3.60	3.90	4.20
e	1.27BSC		
L	0.30	—	1.27

Part No.:	SVD1055SA	Document Type:	Datasheet
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Rev.: 1.2

Revision History:

1. Modify the electrical characteristics and update Fig 5 and 6

Rev.: 1.1

Revision History:

1. Modify the electrical symbol
2. Modify the general description

Rev.: 1.0

Revision History:

1. First release